



IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A computer system, comprising:

- a phase locked loop having a phase-frequency detector, wherein the phase-frequency detector inputs a system clock and generates a chip clock, and wherein the phase-frequency detector generates pulses on a first signal and second signal dependent on a relationship between the system clock and the chip clock; and
- a lock detect indicator that uses the first and second signals to determine whether the phase locked loop is out of lock dependent on whether a pulse on the first signal or the second signal is longer than a predetermined pulse width.

2. (Canceled)

3. (Currently Amended) The computer system of claim 1, wherein the lock detect indicator comprises:

- circuitry that generates a first lock indication pulse if a~~the~~ pulse on the first signal or second signal is longer than a~~the~~ predetermined pulse width;
- circuitry that generates a second lock indication pulse dependent on the first lock indication pulse and a count value; and
- circuitry that uses the second lock indication pulse to dynamically generate a first lock status signal, wherein the first lock status signal is indicative of whether the phase locked loop is out of lock.

4. (Currently Amended) The computer system of claim ~~13~~, wherein the lock detect indicator comprises:

- circuitry that outputs ~~another~~ a second lock status signal, wherein the ~~another~~ second lock status signal is indicative of whether the phase locked loop is out of lock.

5. (Original) The computer system of claim 1, wherein the lock detect indicator comprises:  
circuitry that outputs a past lock status signal, wherein the past lock status signal  
indicates whether the phase locked loop has been out of lock.

<sup>2</sup>  
~~6.~~ (Original) The computer system of claim 1, wherein the lock detect indicator comprises:  
reset circuitry that resets the lock detect indicator dependent on a reset input signal.

7-17. (Canceled)

<sup>6</sup>  
~~18.~~ (Currently Amended) An integrated circuit, comprising:  
generating means for generating a chip clock signal based on a system clock signal,  
wherein the generating means uses a first signal and a second signal to maintain a  
relationship between the chip clock and the system clock;  
detecting means for using the first and second signals to determine whether the  
generating means is out of lock; and  
indicating means for indicating whether the generating means is out of lock dependent on  
whether a pulse on the first signal or the second signal is longer than a  
predetermined pulse width.

<sup>7</sup>  
~~19.~~ (Previously Amended) A method for detecting whether a phase locked loop is out of lock,  
comprising:

generating a first signal and a second signal based on a relationship between a system  
clock and a chip clock used in the phase locked loop;  
determining whether a pulse of the first signal or the second signal is greater than a  
predetermined width;  
generating a pulse on a first lock signal based on the determination; and  
dynamically generating a pulse on a lock status signal dependent on the pulse on the first  
lock signal,

wherein the first signal and the second signal are generated by a phase-frequency detector included in the phase locked loop.

20 - 22. (Cancelled)

*B1 (cont'd)*  
<sup>8</sup>  
~~23.~~ (Original) The method of claim <sup>7</sup>~~19~~, wherein generating the first lock signal comprises:  
using a predetermined delay; and  
generating the pulse on the first lock signal when a pulse on the first signal or the second signal is greater than the predetermined delay.

<sup>9</sup>  
~~24.~~ (Original) The method of claim <sup>7</sup>~~19~~, further comprising generating a lock reset signal, wherein generating the lock reset signal comprises:  
removing glitches on the first lock signal;  
amplifying the pulse on the first lock signal; and  
using the pulse on the first lock signal to selectively reset circuitry used for generating a second lock signal.

<sup>10</sup>  
~~25.~~ (Original) The method of claim <sup>9</sup>~~24~~, wherein generating the lock reset signal is dependent on a reset input signal.

<sup>11</sup>  
~~26.~~ (Original) The method of claim <sup>9</sup>~~24~~, wherein generating the second lock signal comprises:  
counting to a particular value; and  
generating a pulse on the second lock signal when circuitry used for counting to the particular value reaches the particular value.

<sup>12</sup>  
~~27.~~ (Original) The method of claim <sup>9</sup>~~24~~, further comprising:  
generating a pulse on a past lock signal dependent on the second lock signal, wherein the past lock signal indicates whether the phase locked loop has been out of lock.

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